PATENT APPLICATION
Docket No. 9898-208

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ki-Won Choi	Conf. No.	6747
Serial No.	10/055,266	Examiner:	Quang D. Vu
Filed:	January 22, 2002	Art Unit:	2811
For:	SEMICONDUCTOR PACKAGE HAVING CHANGED SUBSTRATE DESIGN USING SPECIAL WIRE BONDING		

DECLARATION UNDER RULE 37 C.F.R. 1.132

I, Ki-Won Choi, declare the following:

1. My relevant educational and occupational background is as follows: I was awarded a B.S. degree in Metallurgical Engineering from Kyungbook University in Korea in 1989. My employment experience spans more than 14 years and involves various semiconductor packaging technologies. In more detail, I have served as a design engineer for Samsung Electronics Inc. in Korea for 14 years. I have been involved in the development of semiconductor memory modules and semiconductor packages. I am currently working as a senior engineer for Samsung Electronics, Inc.

2. I have applied for approximately thirty nine (39) Korean patent applications and three (3) U.S. patent applications. The subject matter of these patent applications relate primarily to semiconductor packaging and memory module technologies.

3. I have extensive training and experience in all aspects of semiconductor packaging and memory module technologies.

4. I have read and understood: U.S. Pat. Serial No. 10/055,266, as filed and as recently amended; U.S. Pat. No. 6,420,789 B1 to Tay et al ("Tay"). I also have read and understood the United States Patent and Trademark Office's Final Office action mailed on July 11, 2003 and the Advisory action mailed on December 12, 2003. Finally, I have read and understand applicants' Amendment and Remarks mailed November 10, 2003.

5. With embodiments of the present invention, even if semiconductor chip design is changed slightly, the existing package substrate can still be used without changing the package substrate design, and without adding a micro-via hole to the substrate 100, by utilizing an added wire bonding unit 114 that is coupled between a redundant bond finger and an added bond finger.

6. In my opinion, Tay does not teach such an added wire bonding unit coupled between a redundant bonder finger and an added bond finger for the reasons set forth below.

7. The line that connects the substrate bond pads 76 and the pad formed along the first inner rectangle, which is alleged by the Examiner as an added wire bonding unit, is not a wire bonding unit. It may be merely a circuit trace for Vcc or ground. If the line connecting all of the substrate bond pads 76 along the direction of the aperture 74 were an added wire bonding unit as alleged by the Examiner, the resulting device would fail because of electrical shorts.

8. Nowhere does Tay teach or disclose that substrate bond pads 76 are connected to another substrate pads using a bonding wire as in the claimed invention. Compare an added wire bonding unit 114 shown in FIG. 6 of the present application and the FIG. 9B of Tay. On the contrary, FIG. 9B of Tay, which is a cross-sectional view of FIG. 9A, does not show that the substrate bond pads 76 are connected to other substrate bond pads using a bonding wire. The text that accompanies FIG. 9A and FIG. 9B is silent about bonding wires

that are connected between the substrate pads formed on the substrate 72.

9. Tay is only directed to stackable BGA chip packages that can be easily burned-in and tested by existing test tooling, e.g., with test pads arranged in a conventional TSOP pin-out pattern. Tay is, however, silent about reducing the cost to change the design of the substrate by utilizing an added wire bonding unit as in the present invention.

10. All of the bond wires 108 disclosed in Tay are merely coupled between die bond pads 106 and substrate bond pads 76, which are, in turn, placed in electrical communication with selective solder balls 80 by circuit traces 78. Nowhere does Tay teach or disclose bonding wires other than the ones connected between the die bond pads 106 and the substrate bond pads 76. Then, the selected solder balls 80 are electrically connected to the test contact pads 84 through second circuit traces 82 so as to provide a conductive path from the test contact pad 84 back to at least one selected substrate bond pad 76.

11. With this arrangement of Tay, semicompleted chip package can then be placed in a conventional burn-in and test apparatus which includes test tooling. In particular, test contact pads are located on the periphery of substrate with complimentarily positioned probes that are preferably arranged in the same TSOP pin-out configuration as the underlying test contact pads 84. That is, there is a corresponding probe 102 for each test contact pad to a respective substrate bond pad 76, which, in turn, is in electrical communication with a respective die bond pad 106 by way of a bond wire 108.

12. Therefore, in Tay, there is absolutely no need for an added wire bonding unit coupled between the redundant bonder finger and the added bond finger, other than the electrical connections described above, unlike the claimed invention.

13. In the present invention, the thickness of the molding compound 210 is thick enough to cover the added wire bonding unit 114 for protection thereof. See FIG. 6 of the

present application. However, in Tay, the molding compound 108 ... not thick enough to c ver any bond wire that connects the substrate bond pads 76 to another substrate bond pads, i.e., the pad formed along the first inner rectangle, if there is any. This demonstrates that there is no such an added wire bonding unit in Tay.

14. For these reasons, in my opinion, Tay does not teach or disclose all of the limitations of the claimed invention, e.g. an added wire bonding unit.

I, the undersigned, declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

DATED this 12 day of Jan., 2004.

Ki-Won Choi